

REMARKS

The Official Action dated August 3, 2004 has been received and their contents reviewed. The Examiner is thanked for reviewing the present application.

By this Amendment, claims 1, 5, 6 and 9 have been amended. Claim 3 was previously cancelled. Accordingly, claims 1, 2 and 4-10 are pending for consideration, of which claims 1, 6 and 9 are independent.

Turning now to the detailed Official Action, claims 1 and 4-10 stand rejected under 35 U.S.C. 102(b) as anticipated by Blocker (U.S. Patent No. 3,969,745 – hereafter Blocker). Further, claim 2 stands rejected under 35 U.S.C. §103(a) as unpatentable over Blocker. These rejections are respectfully traversed for the reasons provided below.

Each of the amended independent claims 1 and 9 recite a semiconductor device including a semiconductor substrate, two semiconductor elements provided on the principal surface of the substrate and multiple through holes which pass in front of the principal surface through the back side of the substrate are provided in a region of the substrate between the two adjacent elements and a conductor film formed directly on the side faces of the through holes. Clearly, Applicants' claimed invention recites a semiconductor device which includes multiple through holes provided between the two adjacent elements so as to increase isolation between the adjacent elements while maintaining the strength of the substrate.

Further, the amended independent claim 6 recites that the first type of through holes is different from the second type of through holes, and the second type of through hole increases isolation between the adjacent elements while maintaining the strength of the substrate. Claim 6 further recites that the second group of through holes are provided in different locations from the first group of through holes.

On the other hand, Blocker discloses that the same type of through holes are respectively provided in a plurality of sources in a semiconductor element (i.e., a field effect transistor), and one through hole is provided between two adjacent elements.

Further, according col. 1, lines 5-11 of Blocker, the through holes in the substrate are metallized to connect to a common conductive layer at the bottom of the substrate to minimize parasite capacitances and inductances to ground. Fig. 3 and col. 3, lines 3-9, for example, of Blocker further disclose that the common conductive metal layer 14 electrically connects to source electrodes 10a-10d by way of solder connections 10j-10n.

Applicants respectfully submit that the through holes of Blocker are actually source electrodes 10a-10d that are interconnected via the metal layer 14 and, hence, the through holes of Blocker are completely different in structure and function than Applicants' claimed through holes, which are not interconnected and which are utilized to increase isolation between the adjacent elements while maintaining the strength of the substrate.

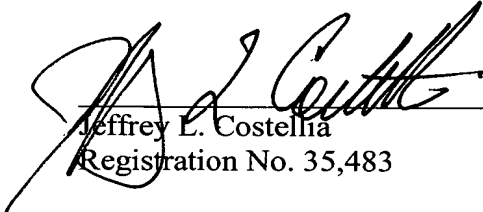
Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Blocker, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1, 2 and 4-10, under 35 U.S.C. §102(b), as anticipated by Blocker is improper.

With respect to the §103(a) rejection of claim 2, this rejection is likewise respectfully traversed for the same reasons set forth above with respect to the §102(b) rejection of its independent claim 1.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Respectfully submitted,



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